## Remarks

The power or attorney and the correspondence address for this application have changed. Please direct future correspondence to the undersigned.

Reconsideration of the application is requested. Claims 4, 6, and 7 stand rejected as unpatentable over Ravanelli in view of Ker. Claims 11-13, 15, 16, and 18-20 stand rejected as unpatentable over Jun in view of Ker.

In response, applicant has amended claims 4 and 11 to clarify their structure. Claim 6 has been amended to correct informalities without narrowing its scope. Claims 22-25 have been added.

Claim 4 now recites a substrate region defined by a uniformly doped region of the substrate extending from the first junction region to the second junction region. Thus in the claimed device, no lightly doped regions (LLDs) exist between the junction regions and the uniformly doped substrate region.

Moreover, claim 4 now recites that the dielectric sidewall spacers overlie the uniformly doped substrate region.

Ravanelli, in contrast, discloses the use of LLDs and therefore lacks the claimed uniformly doped substrate region extending from the first junction region to the second junction region. In Ravanelli a "P-body" region 13 is shown in Fig. 1 between junction region 20 and junction region 18. However, the region 13 does not extend from one junction region to the other. Instead, two N-type regions 14, 15 lie between the region 13 and the respective junction regions 20, 18. In this respect Ravanelli is simply another example of the prior art described in pages 1-3 and shown in Fig. 1 of the pending application.

Ker does not teach positioning sidewall spacers over a uniformly doped substrate region. In Ker's Fig. 3, the sidewall spacers overlie lightly doped regions 118, 120 and 128, 130, not the uniformly doped substrate regions 106 or 108.

Because neither Ravanelli nor Ker teaches or suggests at least these claim limitations, claim 4 and its dependent claims should be patentable over these references.

Amended claim 11 recites more clearly the structure of the claimed input protection circuit, including the transistor distinct from the MOS circuit, the parallel arrangement of the MOS circuit, transistor, and compensating diode, and the positions of the sidewall spacers.

Neither Jun nor Ker shows or suggests at least these limitations, and thus claim 11 and its dependent claims should be patentable over these references.

New claims 22 -25 should be patentable over the cited references for at least the reasons given above.

Applicant submits therefore that the pending claims are in condition for allowance, and such action is requested.

Please call the undersigned if he can be of any further assistance in this case.

Respectfully submitted,

Associate General Counsel, IP

Reg. No. 31325 Customer No. 29416

Lattice Semiconductor Corporation 5555 NE Moore Ct. Hillsboro, OR 97124

Phone: 503-268-8629

Fax: 503-268-8077

mark.becker@latticesemi.com